Notice of Allowability	Application No.	Applicant(s)	
	10/657,196	SERA ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/15/2006 and interview dated 1/16/2007*.

2. ☒ The allowed claim(s) is/are *21-36,40,42,43,46,48 and 53-66*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 09/19/2006
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

THANHHA S. PHAM
PRIMARY EXAMINER

1/16/07

EXAMINER'S AMENDMENT

1. This Office Action is in response to Applicant's Amendment dated 12/15/2006.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Dion Ferguson on 01/16/2007.

The application has been amended as follows:

- Claim 29,

  line 21, change "a" to – the –

  line 36, delete "of said transistors"

  line 40, delete "of said transistors"

- In claim 34,

  line 10, after "the eighth threshold value" delete "of"

- In claim 42,

  line 3, after "the second threshold" insert – value –

- In claim 54,

  line 4, after "second, third and fourth threshold" insert – values –

- In claim 60,

  line 4, after "the second threshold" insert – value –

- In claim 66,

line 1, change "a" to – the --

Allowable Subject Matter

3. Claims 21-36, 40, 42-43, 46, 48, 53-66 are allowed.

4. The following is an examiner's statement of reasons for allowance:

► Recorded Prior Art fails to disclose or suggest the combination structure of a differential amplifier circuit as recited in the base claim 21 including: said differential pair and/or said load element pair comprised of transistors each having relatively low threshold value; and a switch circuit inserted in a current path of said differential stage for controlling an activation and deactivation of said differential stage, said switch circuit comprising at least one transistor which has a threshold value higher than that of the transistors having relatively low threshold value and which is controlled to be on and off by a control signal supplied to a control terminal thereof.

► Recorded Prior Art fails to disclose or suggest the combination structure of a differential amplifier circuit as recited in the base claims 24, 25 including: said first differential pair and/or load element pair including a least a transistor which has relatively low absolute value of a first threshold value; a first switch circuit for controlling an activation and deactivation of said differential stage, wherein said first switch circuit comprises a transistor connected in series with said current source between said differential pair and said second power supply, having a relatively high absolute value of a second threshold value higher than said relatively low absolute value of the first threshold value and comprising a control terminal for receiving a control signal to be

controlled to be on and off, or said first switch circuit comprises said current source comprised of a transistor having a relatively high absolute value of a third threshold value higher than said relatively low absolute value of the first threshold value and including a control terminal for receiving a control signal to be controlled to be on and off.

► Recorded Prior Art fails to disclose or suggest the combination structure of a differential amplifier circuit as recited in the base claim 29 including: said first differential pair and/or said first load element pair being comprised of transistors each having relatively low absolute value of a first threshold value; a first switch circuit for controlling an activation and deactivation of said first differential stage, wherein said first switch circuit comprises a transistor connected in series with said first current source between said first differential pair and said second power supply, having a relatively high absolute value of a third threshold value higher than said relatively low absolute value of the first threshold value and comprising a control terminal for receiving a first control signal to be controlled to be on and off, or said first switch circuit comprises said first current source comprised of a transistor having a relatively high absolute value of a fourth threshold value higher than said relatively low absolute value of the first threshold value and comprising a control terminal for receiving a first bias voltage as said first control signal to be controlled to be on and off.

► Recorded Prior Art fails to disclose or suggest the combination structure of a differential amplifier circuit as recited in the base claim 35 including: said first differential pair and/or said load element pair being comprised of transistors each

having relatively low threshold value; a current source for supplying current to said differential pair wherein said current source is comprised of a transistor having a threshold value higher than that of the transistor having relatively low threshold value and comprising at least a control terminal for receiving a bias voltage as a control signal to be controlled to be on and off.

► Recorded Prior Art fails to disclose or suggest the combination structure of a differential amplifier circuit as recited in the base claim 36 including: said first differential pair and/or said load element pair including at least a transistor which has relatively low absolute value of a first threshold value; a switch circuit for controlling activation and deactivation of said differential amplifier circuit, wherein said switch circuit comprises at least one transistor having a relatively high absolute value of a second threshold value higher than said relatively low absolute value of the first of said transistor and comprising a control terminal for receiving a control signal to be controlled to be on and off.

► Recorded Prior Art fails to disclose or suggest the combination structure of a differential amplifier circuit as recited in the base claim 40 including: said differential pair and/or load element pair including a least a transistor which has relatively low absolute value of a first threshold value; a switch circuit inserted in a current path of said differential stage for controlling an activation and deactivation of said differential stage, said switch circuit comprising at least one transistor which has a relatively high absolute value of a second threshold value higher than said relatively low absolute

value of the first threshold value and which is controlled to be on and off by a control signal supplied to a control terminal thereof.

► Recorded Prior Art fails to disclose or suggest the combination structure of a differential amplifier circuit as recited in the base claim 63 including: a current source for supplying a current to said differential pair; said differential pair and/or load element pair including a least a transistor which has relatively low absolute value of a first threshold value; wherein said current source is comprised of a transistor having a relatively high absolute value of a second threshold value higher than said relatively low absolute value of the first threshold value and comprising a control terminal for receiving a bias voltage as a control signal to be controlled to be on and off.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TSP

THANHHA S. PHAM
PRIMARY EXAMINER

1/16/07